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10EE764

Seventh Semester B.E. Degree Examination, Feb./Mar.2022
VLSI Circuits and Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the fabrication steps of P-well CMOS process. **(10 Marks)**

b. Explain the transistor action of enhancement mode nMOS transistor for different values of V_{gs} and V_{ds}. **(06 Marks)**

c. Compare CMOS and BJT technologies. **(04 Marks)**

2 a. Derive an expression for the drain current I_{ds} of an enhancement mode nMOS transistor for the following regions:
(i) Linear (ii) Saturation. (iii) Cutoff.
Also plot I_{ds}, V_s V_{ds} and mark the above regions. **(10 Marks)**

b. Explain the five regions of operations of CMOS inverter transfer characteristics. **(10 Marks)**

3 a. Draw the circuit diagram of a 2-input CMOS NAND gate along with stick diagram. Explain the working of the circuit. **(08 Marks)**

b. Indicate and draw design rule for diffusion layers and metal layers. **(06 Marks)**

c. Distinguish buried and butting contacts with suitable diagrams. **(06 Marks)**

4 a. Explain the terms : (i) Rise time (ii) Full time. Derive the equations for the rise time (t_r) and fall time (t_f) of CMOS inverter. Also derive the conditions for $t_r = t_f$. **(10 Marks)**

b. Derive the expression for total delay for N stages of nMOS and CMOS inverters in terms of width factor f and delay T. **(06 Marks)**

c. Write a short note on choice of layers. **(04 Marks)**

PART – B

5 a. Obtain the scaling factor for the following parameters:
(i) Gate Capacitance (C_g)
(ii) Current Density (J)
(iii) Maximum Operating Frequency (f_0)
(iv) Power speed product (P_T)
(v) Gate delay (T_d) **(10 Marks)**

b. Discuss the limitation of scaling on substrate doping and depletion width. **(10 Marks)**

6 a. Explain the working of switch logic, pass-transistor and transmission gates with their merits and demerits. **(10 Marks)**

b. Explain the structural design concept using bus arbitration logic as an example. **(10 Marks)**

7 a. What are the general considerations to be followed in designing a subsystem? **(08 Marks)**

b. What are the basic requirements of a shifter? Explain with an example of 4×4 cross bar switch. What are the drawbacks of this basic switch and how is it overcome? **(12 Marks)**

8 a. Design a 4-bit adder and then show how it can be used to implement the ALU functions. **(12 Marks)**

b. Explain the arrangement of a 4-bit serial-parallel multiplier. **(08 Marks)**

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